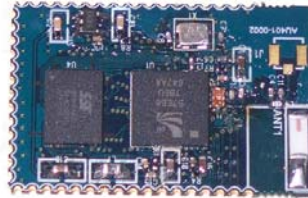


Bluetooth V2.0 Class 2 module

Product datasheet



General Description

AUBTM-23 is Bluetooth Core V2.0 compliant module. The module is designed to be embedded in a host system which requires cable replacement function. Typically the module could interface with a host through the UART port.

The module could be used in many different application, e.g.:

- High Quality Stereo Wireless Headsets
- High Quality Mono Headsets
- Hands-Free Car Kits
- Wireless Speakers
- VOIP Handsets
- Analogue and USB Multimedia Dongles
- Bluetooth-Enabled Automotive Wireless Gateways

Key Specification

- Fully Qualified Bluetooth v2.0+EDR system
- Handsfree/Headset profile, A2DP, AVRCP, OPP support
- Enhanced Audibility and noise cancellation (with additional DSP software)
- Support UART,USB,PCM,I2C interface to host system
- Integrated battery charger
- Support for 802.11 Co-existence
- RoHS Compliant

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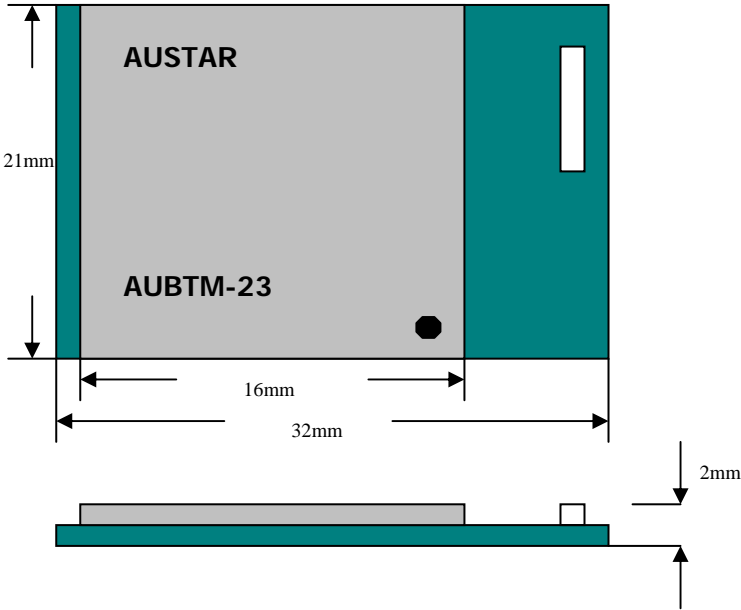
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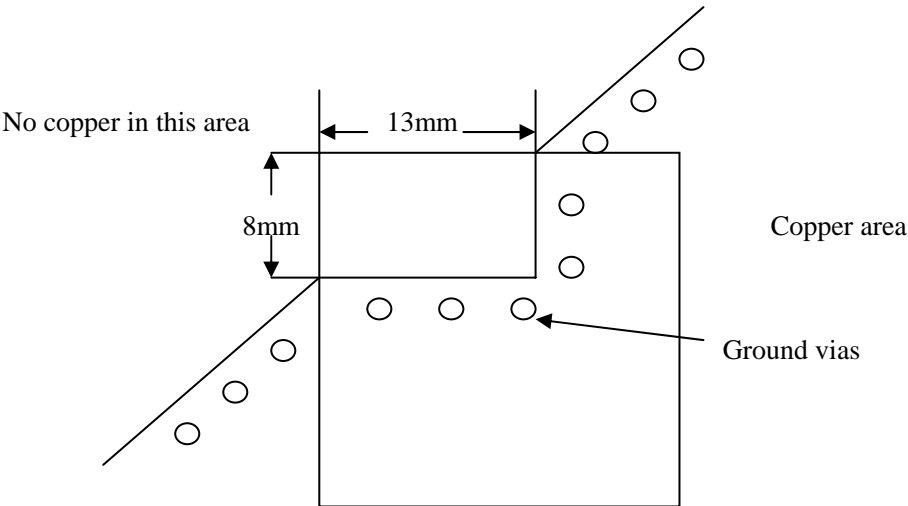
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1 Structure



2 PCB layout specification



3 Package Information:

3.1 Pinout Diagram

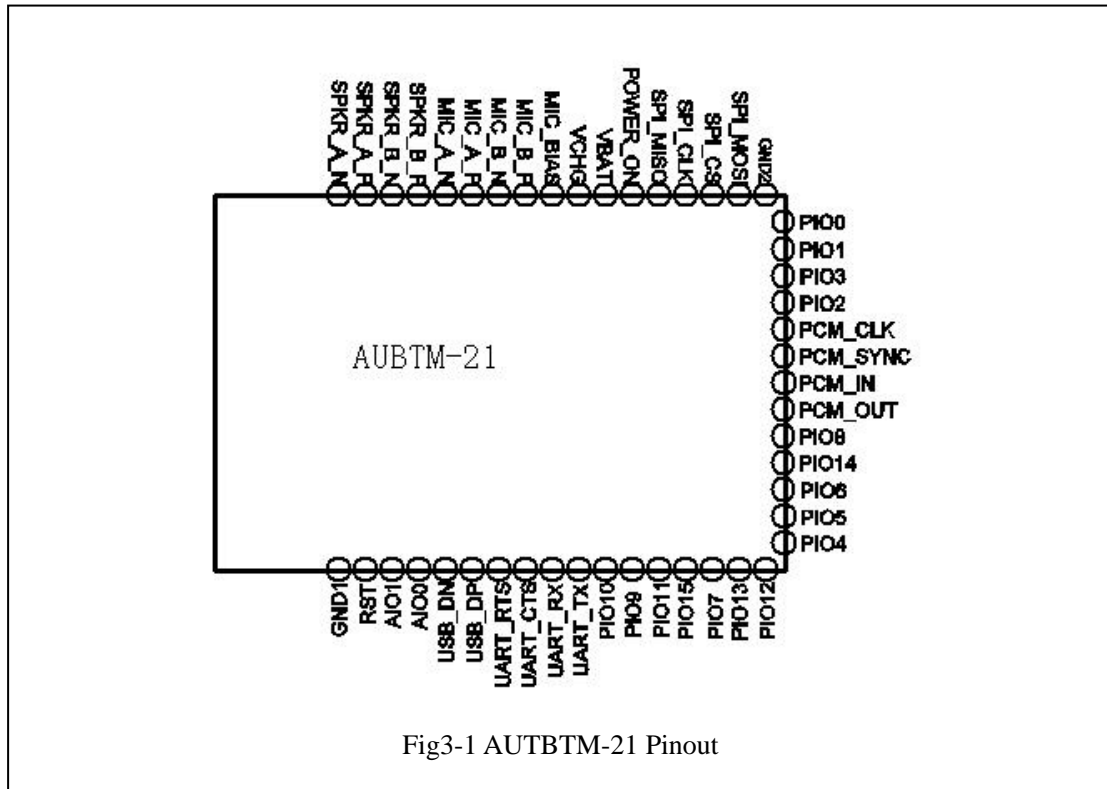


Fig3-1 AUBTM-21 Pinout

3.2 Terminal Functions

Pin Number	Pin name	I/O	
1.	GND1		Ground
2.	RST		Reset
3.	AIO1		Analog input/output channel 1
4.	AIO0		Analog input/output channel 0
5.	USB_DN		USB data negative
6.	USB_DP		USB data positive
7.	UART_RTS		UART RTS
8.	UART_CTS		UART CTS
9.	UART_RX		UART RX
10.	UART_TX		UART TX

11.	PIO10		Digital input/output port 10
12.	PIO9		Digital input/output port 9
13.	PIO11		Digital input/output port 11
14.	PIO15		Digital input/output port 15
15.	PIO7		Digital input/output port 7
16.	PIO13		Digital input/output port 13
17.	PIO12		Digital input/output port 12
18.	PIO4		Digital input/output port 4
19.	PIO5		Digital input/output port 5
20.	PIO6		Digital input/output port 6
21.	PIO14		Digital input/output port 14
22.	PIO8		Digital input/output port 8
23.	PCM_OUT		Synchronous 8 kbps data out (internal Pull down)
24.	PCM_IN		Synchronous 8 kbps data in (internal Pull down)
25.	PCM_SYNC		Synchronous data strobe (internal pull-down)
26.	PCM_CLK		Synchronous data clock (internal pull-down)
27.	PIO2		Digital input/output port
28.	PIO3		Digital input/output port
29.	PIO1		Digital input/output port
30.	PIO0		Digital input/output port
31.	GND2		Ground
32.	SPI_MOSI		SPI data input (pull down)
33.	SPI_CS		Chip selection for SPI (internal pull up, active low)
34.	SPI_CLK		SPI Clock (internal pull down)
35.	SPI_MISO		SPI data output (pull down)
36.	POWER_ON		Power enable
37.	VBAT		Battery in
38.	VCHG		Charging Voltage
39.	MIC_BIAS		Microphone bias
40.	MIC_B_P		Microphone B positive
41.	MIC_B_N		Microphone B negative
42.	MIC_A_P		Microphone A positive
43.	MIC_A_N		Microphone A negative
44.	SPKR_B_P		Speaker B positive
45.	SPKR_B_N		Speaker B negative
46.	SPKR_A_P		Speaker A positive
47.	SPKR_A_N		Speaker A negative

4 Device Terminal Description

4.1 Audio Input/output

AUBTM-23 audio input receives its analogue input signal from pins AUDIO_IN_P_LEFT and AUDIO_IN_N_LEFT. The input can be configured to be either single ended or fully differential. It can be programmed for either microphone or line input and has a 3-bit digital gain setting of the input-amplifier in 3dB steps to optimize it for the use of different microphones.

AUBTM-23 has a class-AB amplifier as the audio output-stage and is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of $32\ \Omega$ and 500pF with a typical THD+N of -74dBc. The output is available as a differential signal between AUDIO_OUT_N_LEFT and AUDIO_OUT_P_LEFT for the left channel ; and between AUDIO_OUT_N_RIGHT and AUDIO_OUT_P_RIGHT for the right channel. The output is capable of driving a speaker directly if its impedance is at least $16\ \Omega$ if only one channel is connected or an external regulator is used.

4.2 UART

AUBTM-23 Universal Asynchronous Receiver Transmitter (UART) interface provides a simple mechanism for communicating with other serial devices.

Four signals are used to implement the UART function. When AUBTM-23 is connected to another digital device, RXD and TXD transfer data between the two devices. The remaining two signals, NCTS and NRTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD.

Parameter		Possible Values
Baud Rate	Minimum	1200 Baud ($\leq 2\%$ Error)
	Maximum	9600 Baud ($\leq 1\%$ Error)
		1.5MBaud ($\leq 1\%$ Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per channel		8

Possible UART Settings (1)

(1) UART settings are set during factory calibration. Customer should provide desired

configuration before purchasing.

4.3 PIO

AUBTM-23 provides 16 lines of programmable bi-directional input/outputs (I/O) are provided. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

4.4 AIO

AUBTM-23 has 2 general purpose analogue interface pins, AIO[0], AIO[1] . AIO pins are mainly used as inputs of internal A/D converters. Typical use of these pins are monitoring the battery level.

4.5 USB

AUBTM-23 contains a full speed (12Mbits/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v1.2 or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a Master/Slave oriented system (in common with other USB peripherals), AUBTM-23 only supports USB Slave operation.

4.6 Power control

AUBTM-23 contains built-in DC/DC regulator to provide power supply for the module. A battery or an external DC power supply could be connected with VBAT to power the module. Pin Power_on is used to enable the module, allowing the device to boot up. When Power_on is high, the internal power supply is enabled. The firmware is then about to latch the internal regulator and the Power_on pin could be released. Power_on has a logic threshold of around 1V, and have weak pull-downs. It can tolerate voltages up to 4.9V, so it may be connected directly to a battery to enable the device.

4.7 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, VBAT, with the switch mode regulator; however it may be used in conjunction with either of the high voltage regulators on the device. The constant current level can be varied to allow charging of different capacity batteries. The charger circuit requires configuration and calibration settings which are stored in the device. To ensure these are set, the circuit enables the active regulators whenever it enters ‘fast-charge’ mode so that the device will boot-up and run the charger configuration firmware.

Firmware can detect, using an internal status bit, when the charger is powered.

When the charger supply is not connected to VCHG, the terminal must be left open circuit.

5 Electrical specification:

5.1 Radio Characteristics

Parameter	Min	Typ	Max	Unit
Output Power	-	4	-	dBm
Power control range	14			dB
Power control step	2		8	dB
Operation Current		70	110	mA
Sensitivity		-80	-82	dBm

5.2 Power Control

Parameter	Min	Typ	Max	Unit
Supply Voltage(VBAT)	2.7	-	4.5	V
Battery Charger Input Voltage	4.5		6.5	V

5.3 Digital Terminal Input voltage

Parameter	Min	Typ	Max	Unit
VIL input logic level low		-0.4	+0.8	V
VIH input logic level high	2.0625		3.6	V

5.4 Digital Terminal Output voltage

Parameter	Min	Typ	Max	Unit
VOL output logic level low			0.125	V
VOL output logic level high	2.475		3.3V	V

5.5 Input and Tri-state Current with:

Parameter	Min	Typ	Max	Unit
Strong pull-up	-100	-40	-10	μ A
Strong pull-down	+10	+40	+100	μ A

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Weak pull-up	-5.0	-1.0	-0.2	μ A
Weak pull-down	+0.2	+1.0	+5.0	μ A
I/O pad leakage current	-1	0	+1	μ A
CI Input Capacitance	1.0	-	5.0	pF

5.6 USB Terminals Characteristics

Parameter	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input threshold				
VIL input logic level low	-	-	0.99	V
VIH input logic level high	2.31	-	-	V
Input leakage current				
VSS < VIN < VDD	-1	1	5	μ A
CI Input capacitance	2.5	-	10.0	pF
Output Voltage levels to correctly terminated USB Cable				
VOL output logic level low	0.0	-	0.2	V
VOH output logic level high	2.8	-	3.3	V

5.7 Auxiliary ADC

Parameter	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Input voltage range (LSB size = 3.3/255)	0	-	3.3	V
Accuracy(Guaranteed monotonic)	INL	-1	1	LSB
	DNL	0	1	LSB
Offset	-1	-	1	LSB
Gain Error	-0.8	-	0.8	%
Input Bandwidth	-	100	-	kHz
Conversion time	-	2.5	-	μ s
Sample rate(2)	-	-	700	Samples/s

5.8 Audio Input, Microphone Amplifier

Parameter	Min	Typ	Max	Unit
Input full scale at maximum gain	-	4	-	mV rms
Input full scale at minimum gain	-	400	-	mV rms

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Gain resolution	-	3	-	dB
Distortion at 1kHz	-		-74	dB
Input referenced rms noise	-	8	-	μ V rms
3dB Bandwidth	-	17	-	kHz
Input impedance	-	20	-	k Ω
THD+N (microphone input) @ 30mV rms input	-	-66	-	dB
THD+N (line input) @ 300mV Ω input(9)	-	-74	-	dB

5.9 Audio Output, Speaker Output

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Allowed Load		Resistive	16	-	O.C.	Ω
		Capacitive	-	-	500	pF
Max output voltage		RL=600 Ω	-	2.0	-	V pk-pk
Max output current		RL=22 Ω	-	75	-	mA
Total Harmonic Distortion plus Noise	THD+N	fIN=1kHz, BW=22Hz to 22kHz RL=600 Ω	-	0.015	-	%
Output noise relative to full scale	SNR	A Weighted, Po=digital silence, RL=600 Ω , BW=22Hz to 22kHz	-	-91	-	dB
Channel Separation (Crosstalk)	CS	fIN=10kHz, analogue output set to maximum gain	-	-	-60	dB
Power Supply Rejection Ratio	PSRR	Vripple=200mVpk-pk sinewave, 10kHz at VREG_IN. 2.3V \leq VREG_IN \leq 4.1V, analogue output set to maximum gain	-	TBD	-	dB
Second Harmonic Level		1kHz sinewave, 1dB below full scale 600 Ω	-	<-95	-	dB

AUBTM-23

Third Harmonic Level		1kHz sinewave, 1dB below full scale 600Ω	-	-95	-	dB
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6 Manual Soldering

TBA

6.1 Reflow soldering

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimize the out gassing of the flux.
3. Reflow Zone - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.
5. Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%

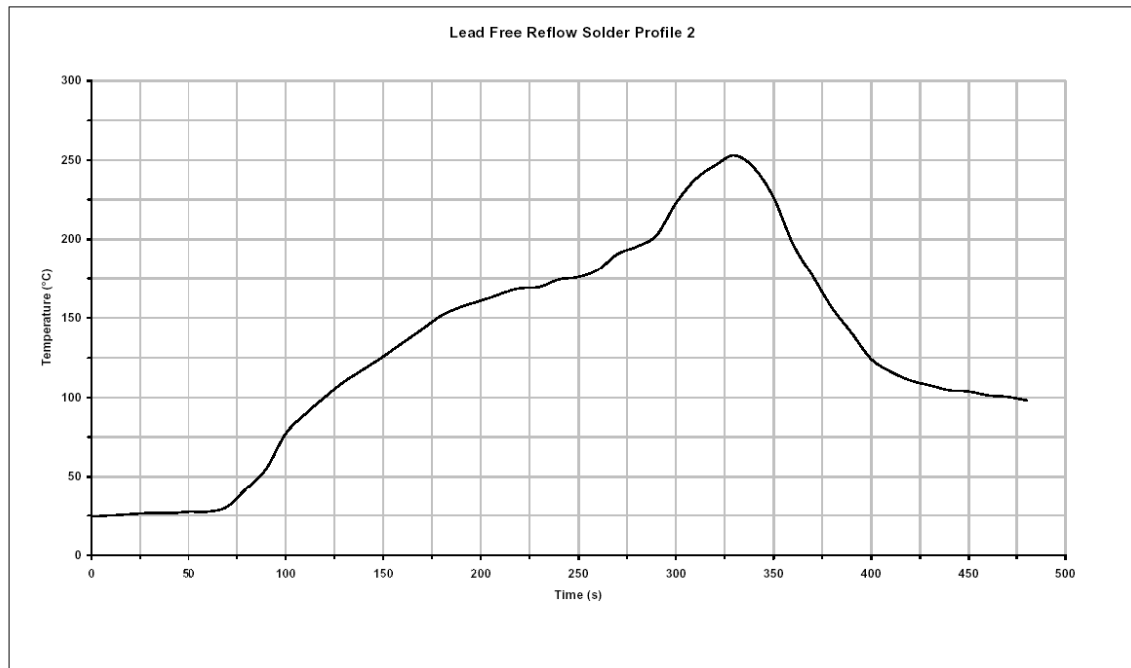


Figure 34: Reflow solder profile

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 260°C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260°C.

7 Referenced schematic design

Revision History

DATE	VERSION	DESCRIPTION
Jul 04, 2009	a	Preliminary publication